WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a memory unit having a plurality of addresses for temporarily storing a data signal;

a data signal providing unit for providing said data signal to said memory unit;

a driving unit for generating a control signal for controlling a functional element based on said data signal read out from said memory unit and providing said control signal to said functional element; and

a data-update control unit for successively providing an identical data signal over a plurality of times from an identical address in said memory unit.

2. The semiconductor device as set forth in Claim 1,wherein said data-update control unit causes said data signal providing unit to suspend the operation of providing a data signal, in order to keep said data signal stored in said memory unit from being updated when successively providing the identical data signal to said functional element.

3. The semiconductor device as set forth in Claim 1, wherein said data-update control unit causes said data signal providing unit to shut off a data signal transmission route from said data signal providing unit to said memory unit, in order to keep said data signal stored in said memory unit from being updated when successively providing the identical data signal to said functional element.

4. A semiconductor device comprising:

a memory unit having a plurality of addresses for temporarily storing a data signal;

a driving unit for selecting a control signal input from outside for controlling a functional element based on said data signal read out from said memory unit and providing said control signal to said functional element; and

a data-update control unit for successively providing an identical signal over a plurality of times from an identical address in said memory unit.

5. A semiconductor device comprising:

a memory unit having a plurality of addresses for temporarily storing a data signal;

a first driving unit for outputting to a functional element a signal for selecting, based on said data signal read out from said memory unit, a control signal input from outside for controlling said functional element;

a second driving unit for providing said control signal to said functional element; and

a data-update control unit for successively providing an identical signal over a plurality of times from an identical address in said memory unit.

6. The semiconductor device as set forth in Claim 1, wherein said driving unit and said memory unit constitute a combined unit.

7. The semiconductor device as set forth in Claim 4, wherein said driving unit and said memory unit constitute a combined unit.

8. The semiconductor device as set forth in Claim 5, wherein said driving unit and said memory unit constitute a combined unit.

9. The semiconductor device as set forth in Claim 1, wherein said driving unit, said functional element and said memory unit constitute a combined unit.

10. The semiconductor device as set forth in Claim 4, wherein said driving unit, said functional element and said memory unit constitute a combined unit.

11. The semiconductor device as set forth in Claim 5, wherein said driving unit, said functional element and said memory unit constitute a combined unit.

12. The semiconductor device as set forth in Claim 1, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the semiconductor device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

13. The semiconductor device as set forth in Claim 4, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the semiconductor device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

14. The semiconductor device as set forth in Claim 5, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the semiconductor device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

15. The semiconductor device as set forth in Claim 1, further comprising a level converter for converting an amplitude of said data signal input to said memory unit to a desired amplitude.

16. The semiconductor device as set forth in Claim 4, further comprising a level converter for converting an amplitude of said data signal input to said memory unit to a desired amplitude.

17. The semiconductor device as set forth in Claim 5, further comprising a level converter for converting an amplitude of said data signal input to said memory unit to a desired amplitude.

18. The semiconductor device as set forth in Claim 1, to which a serial signal is to be input, further comprising serial/parallel converter for converting the input serial data signal into a parallel signal.

19. The semiconductor device as set forth in Claim 4, to which a serial signal is to be input, further comprising serial/parallel converter for converting the input serial data signal into a parallel signal.

20. The semiconductor device as set forth in Claim 5, to

which a serial signal is to be input, further comprising serial/parallel converter for converting the input serial data signal into a parallel signal.

21. The semiconductor device as set forth in Claim 1, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

22. The semiconductor device as set forth in Claim 4, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

23. The semiconductor device as set forth in Claim 5, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

24. The semiconductor device as set forth in Claim 1, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

25. The semiconductor device as set forth in Claim 4, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

26. The semiconductor device as set forth in Claim 5, wherein

at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

27. The semiconductor device as set forth in Claim 24, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

28. The semiconductor device as set forth in Claim 25, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

29. The semiconductor device as set forth in Claim 26, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

30. An image output device provided with an injector for firing a droplet for printing, comprising:

a memory unit for temporarily storing a data signal to be provided to said injector;

a driving unit for reading out said data signal stored in said memory unit, generating a control signal for controlling said injector and driving said injector based on said control signal; and

a data-update control unit for causing a data signal providing unit to suspend outputting said data signal to said memory unit when successively providing an identical control signal to said injector over a plurality of times, so that said memory unit does not update said data signal stored therein.

31. An image output device provided with an injector for firing a droplet for printing, comprising:

a memory unit for temporarily storing a data signal for selecting a driving waveform to be provided to said injector;

a driving unit for reading out said data signal stored in said memory unit, selecting said driving waveform input from outside based on said data signal and driving said injector based on said selected driving waveform; and

a data-update control unit for causing a data signal providing unit to suspend outputting said data signal to said memory unit when successively providing an identical control signal to said injector over a plurality of times, so that said memory unit does not update said data signal stored therein.

32. An image output device provided with an injector for firing a droplet for printing, comprising:

a memory unit for temporarily storing a data signal for selecting a driving waveform to be provided to said injector;

a first driving unit for reading out said data signal stored in said memory unit, and outputting to said injector a signal for selecting based on said data signal said driving waveform input from outside

a second driving unit for providing said selected driving waveform to said injector; and

a data-update control unit for causing a data signal providing unit to suspend outputting said data signal to said memory unit when successively providing an identical control signal to said injector over a plurality of times, so that said memory unit does not update said data signal stored therein.

33. The image output device as set forth in Claim 30, wherein

said driving unit and said memory unit may constitute a combined unit.

34. The image output device as set forth in Claim 31, wherein said driving unit and said memory unit may constitute a combined unit.

35. The image output device as set forth in Claim 32, wherein said driving unit and said memory unit may constitute a combined unit.

36. The image output device as set forth in Claim 30, wherein said driving unit and said memory unit constitute a combined unit.

37. The image output device as set forth in Claim 31, wherein said driving unit and said memory unit constitute a combined unit.

38. The image output device as set forth in Claim 32, wherein said driving unit and said memory unit constitute a combined unit.

39. The image output device as set forth in Claim 30, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the image output device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

40. The image output device as set forth in Claim 31, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said

data signal to the image output device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

41. The image output device as set forth in Claim 32, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the image output device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

42. The image output device as set forth in Claim 30, further comprising a level converter for converting an amplitude of said data signal input into the image output device to a desired amplitude.

43. The image output device as set forth in Claim 31, further comprising a level converter for converting an amplitude of said data signal input into the image output device to a desired amplitude.

44. The image output device as set forth in Claim 32, further comprising a level converter for converting an amplitude of said data signal input into the image output device to a desired amplitude.

45. The image output device as set forth in Claim 30, to

which said data signal is to be input in a form of a serial signal, further comprising:

an S/P converter for converting said input serial data signal into a parallel signal.

46. The image output device as set forth in Claim 31, to which said data signal is to be input in a form of a serial signal, further comprising:

an S/P converter for converting said input serial data signal into a parallel signal.

47. The image output device as set forth in Claim 32, to which said data signal is to be input in a form of a serial signal, further comprising:

an S/P converter for converting said input serial data signal into a parallel signal.

48. The image output device as set forth in Claim 45, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

49. The image output device as set forth in Claim 46, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

50. The image output device as set forth in Claim 47, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

51. The image output device as set forth in Claim 47, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

52. The image output device as set forth in Claim 48, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

53. The image output device as set forth in Claim 49, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

54. The image output device as set forth in Claim 51, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

55. The image output device as set forth in Claim 52, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

56. The image output device as set forth in Claim 53, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

57. Driving method of a functional element comprising the steps of:

temporarily storing a data signal for controlling a functional element in a memory unit;

reading out said data signal and transferring said data signal to said functional element; and

transferring said data signal for controlling the functional element from an identical address of said memory unit instead of updating said data signal retained in said memory unit, in case where it is predetermined that the identical data signal to said data signal stored in said memory unit is to be successively used.

58. Manufacturing method of a semiconductor device comprising the step of forming a thin film transistor circuit including a memory unit for temporarily storing a signal for controlling an element array, an element array and a driving unit for driving said element array on a same insulating substrate through one and the same process.

59. The manufacturing method as set forth in Claim 58, wherein said insulating substrate is a glass substrate.

60. Manufacturing method of an image output device provided with a printhead, comprising the step of forming on a same insulating substrate a thin film transistor circuit including a memory unit for temporarily storing a control signal for an ink injector provided in said printhead, an injector and a driving unit for driving said injector, through one and the same process.

61. The manufacturing method as set forth in Claim 60, wherein said insulating substrate is a glass substrate.